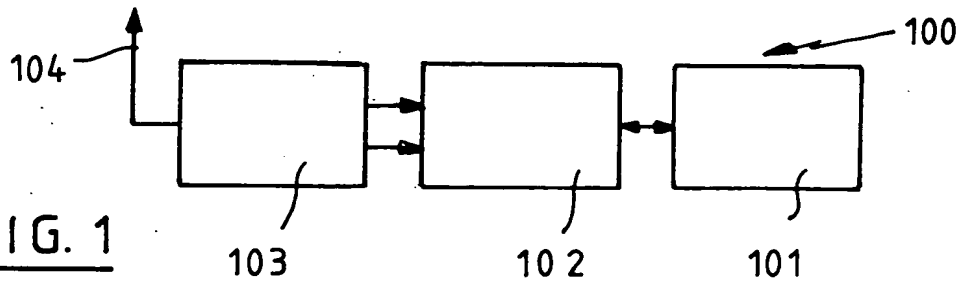

104
100
103
102
101

FIG. 1

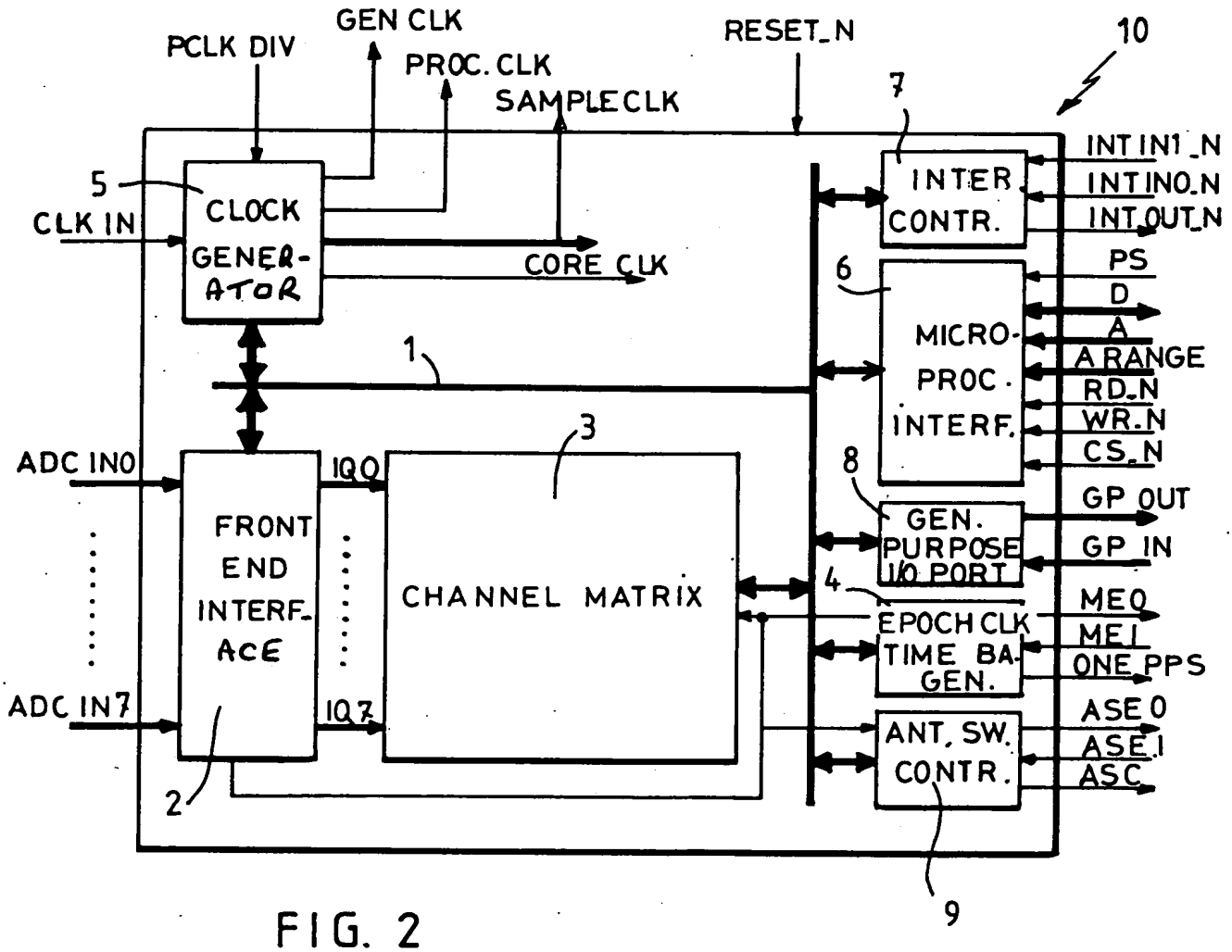

PCLK DIV
GEN CLK
PROC. CLK
SAMPLE CLK
RESET_N
10
7
INTERR CONTR.
INT IN1_N
INT IN0_N
INT OUT_N
5
CLK IN
CLOCK GENER-ATOR
CORE CLK
6
PS
D
A
A RANGE
RD_N
WR_N
CS_N
MICRO-PROC. INTERF.
1
3
ADC IN0
100
FRONT END INTERF-ACE
CHANNEL MATRIX
8
GEN. PURPOSE I/O PORT
GP OUT
GP IN
4
EPOCH CLK
TIME BA. GEN.
ME0
ME1
ONE PPS
ADC IN7
107
ANT. SW. CONTR.
ASE 0
ASE 1
ASC
2
9

FIG. 2

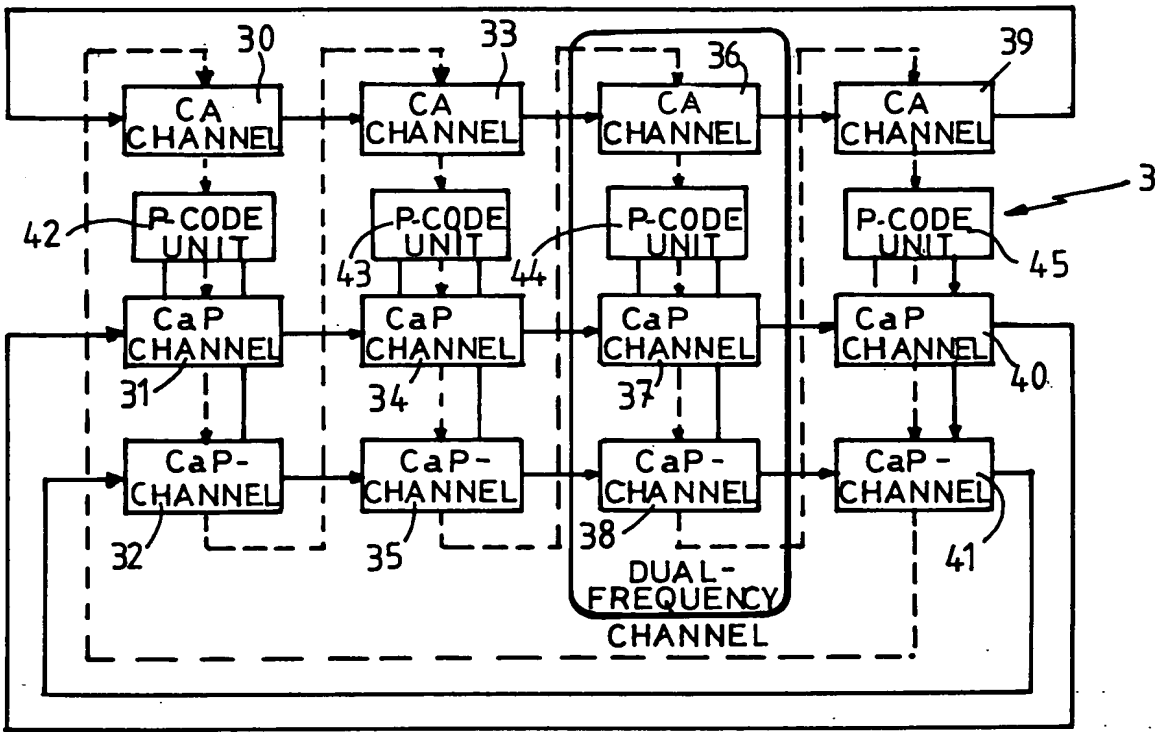

30
33
36
39
CA CHANNEL
CA CHANNEL
CA CHANNEL
CA CHANNEL
3
42
P-CODE UNIT
43
P-CODE UNIT
44
P-CODE UNIT
P-CODE UNIT
45
CaP CHANNEL
CaP CHANNEL
CaP CHANNEL
CaP CHANNEL
31
34
37
40
CaP-CHANNEL
CaP-CHANNEL
CaP-CHANNEL
CaP-CHANNEL
32
35
38
41
DUAL-FREQUENCY CHANNEL

FIG. 3

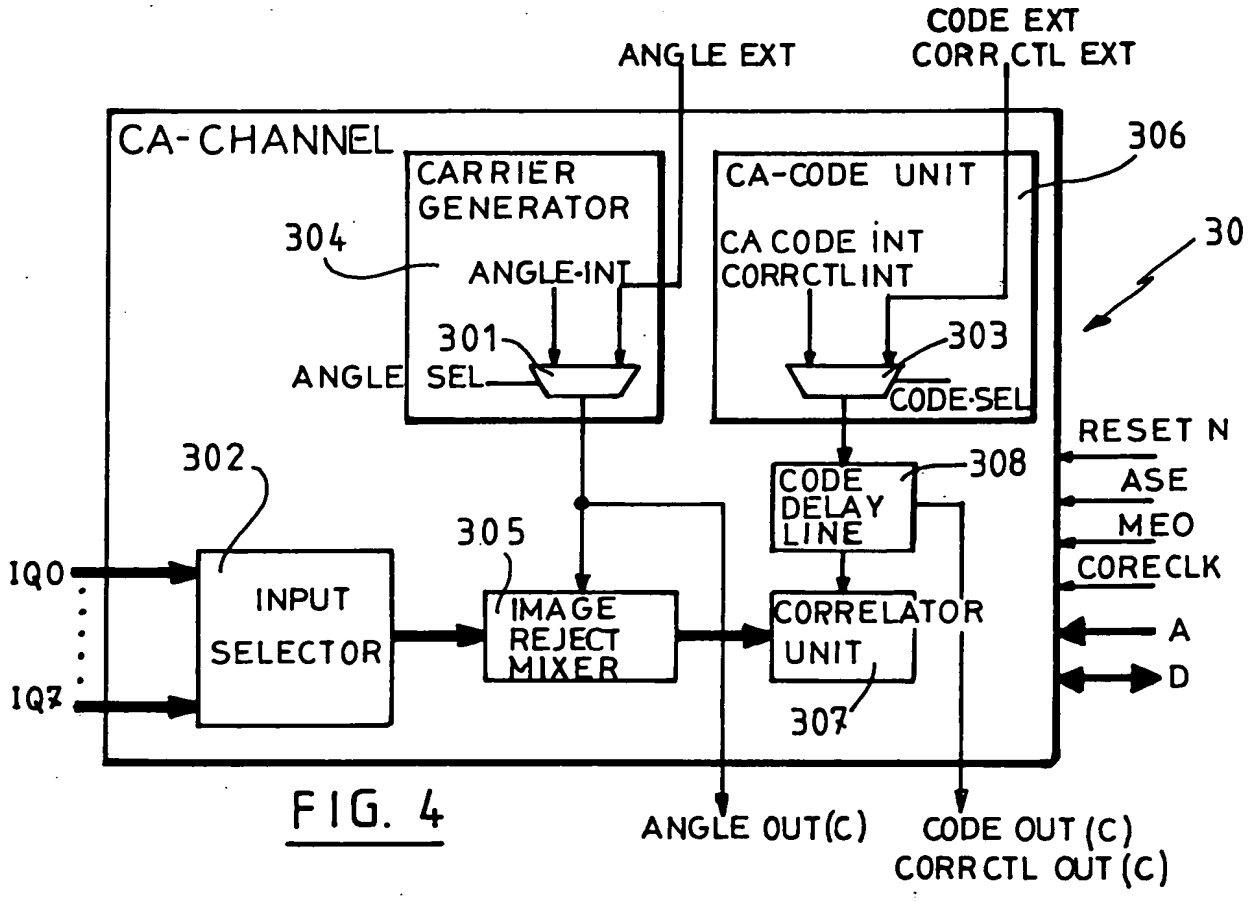

ANGLE EXT
CODE EXT
CORR CTL EXT
CA-CHANNEL
CARRIER GENERATOR
304
ANGLE-INT
301
ANGLE SEL
CA-CODE UNIT
306
CA CODE INT
CORRCTLINT
303
CODE-SEL
30
RESET N
ASE
MEO
CORECLK
A
D
302
IQ0
IQ7
INPUT SELECTOR
305
IMAGE REJECT MIXER
CODE DELAY LINE
308
CORRELATOR UNIT
307
ANGLE OUT(C)
CODE OUT (C)
CORRCTL OUT (C)

FIG. 4

FIG. 5

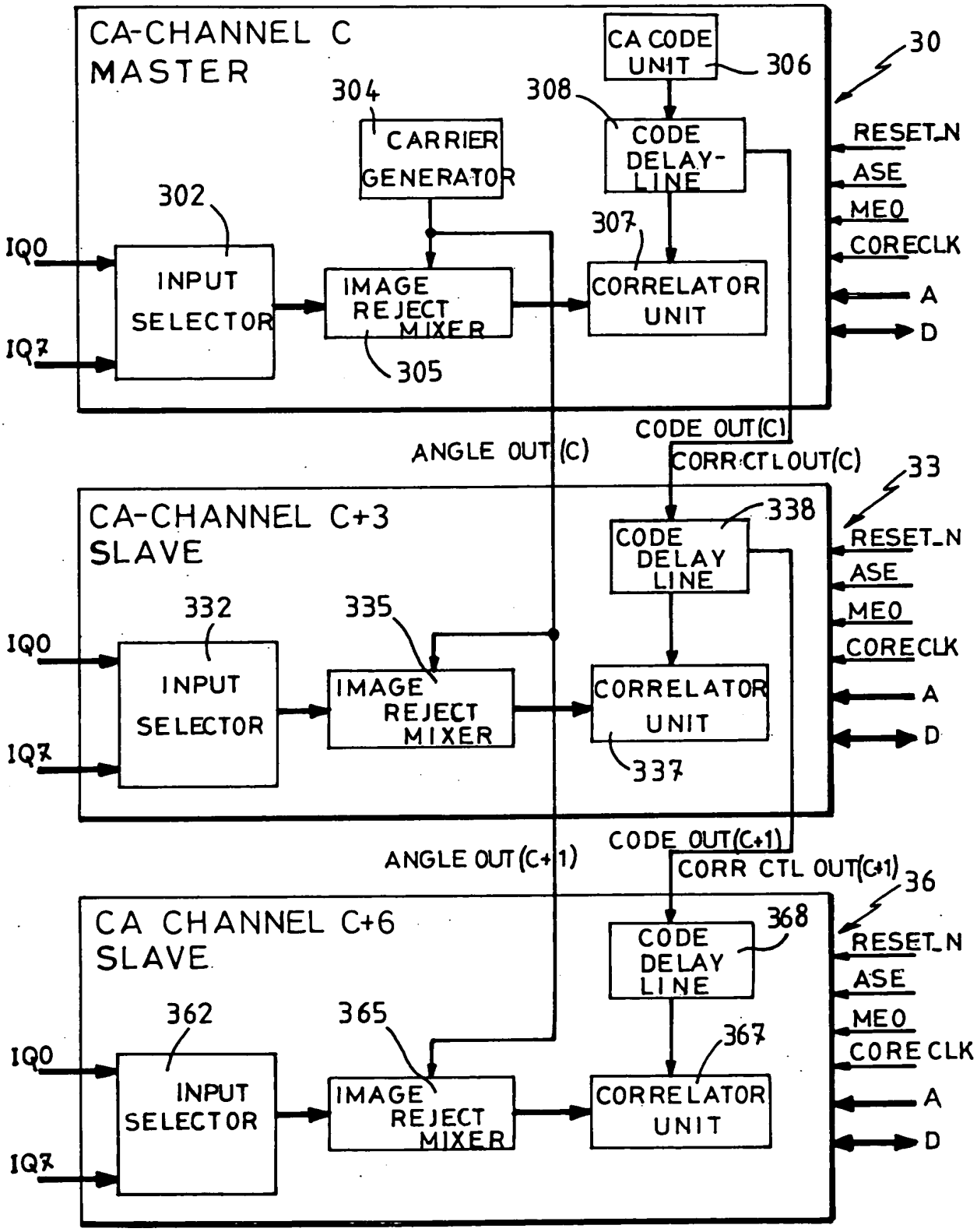
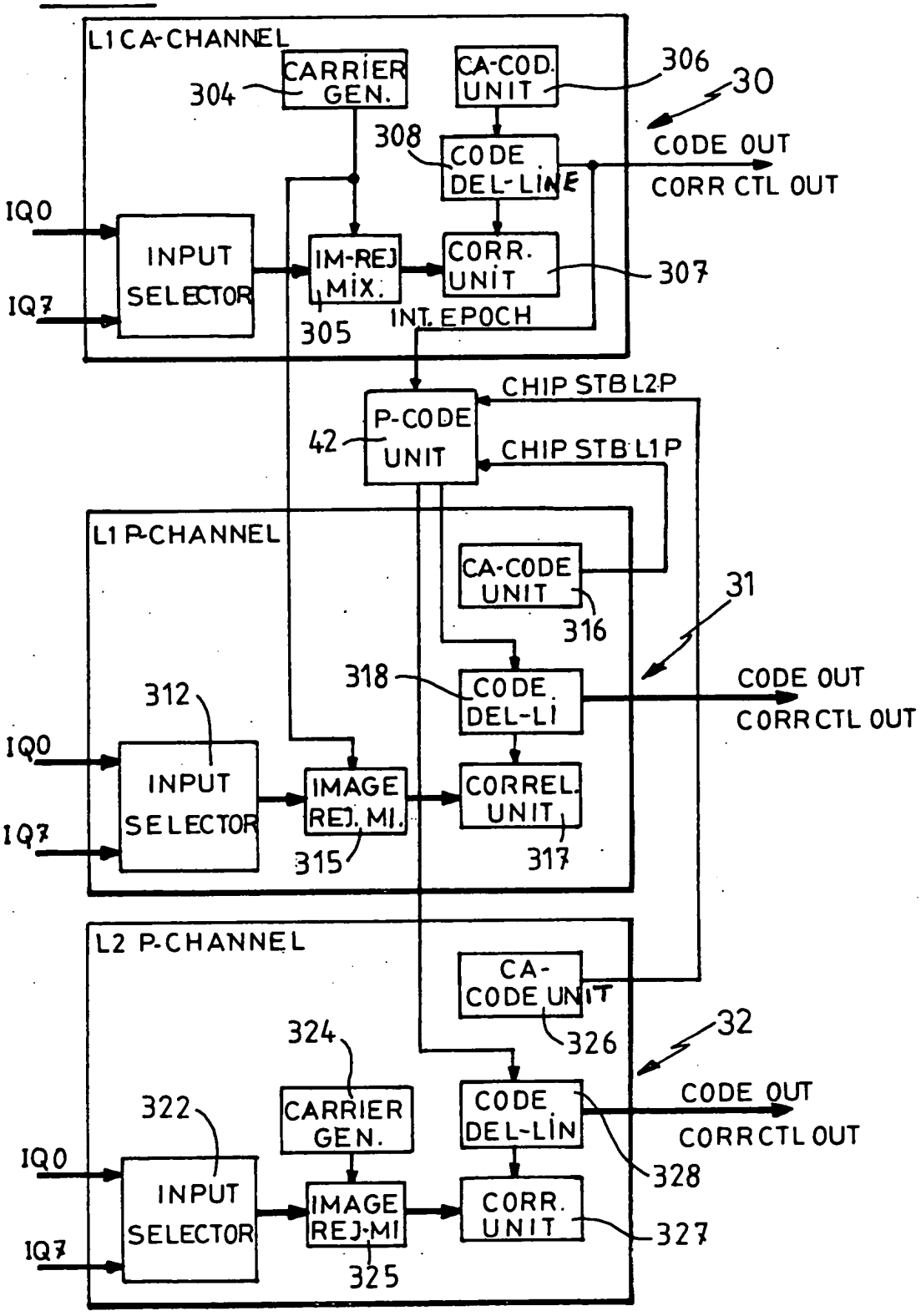

CA-CHANNEL C
MASTER
CA CODE UNIT
306
30
304
308
CARRIER GENERATOR
CODE DELAY-LINE
RESET_N
ASE
MEO
CORECLK
A
D
302
307
IQ0
IQ7
INPUT SELECTOR
IMAGE REJECT MIXER
CORRELATOR UNIT
305
CODE OUT(C)
ANGLE OUT(C)
CORR CTL OUT(C)
33
CA-CHANNEL C+3
SLAVE
338
CODE DELAY LINE
332
335
INPUT SELECTOR
IMAGE REJECT MIXER
CORRELATOR UNIT
337
CODE OUT(C+1)
ANGLE OUT(C+1)
CORR CTL OUT(C+1)
36
CA CHANNEL C+6
SLAVE
368
CODE DELAY LINE
362
365
367
INPUT SELECTOR
IMAGE REJECT MIXER
CORRELATOR UNIT

FIG. 6


L1 CA-CHANNEL
CARRIER GEN.
304
CA-COD. UNIT
306
30
CODE OUT
CORR CTL OUT
308
CODE DEL-LINE
IQ0
IQ7
INPUT SELECTOR
IM-REJ MIX.
305
CORR. UNIT
307
INT. EPOCH
CHIP STB L2P
P-CODE UNIT
42
CHIP STB L1P
L1 P-CHANNEL
CA-CODE UNIT
316
31
318
CODE DEL-LI
CODE OUT
CORR CTL OUT
312
IQ0
IQ7
INPUT SELECTOR
IMAGE REJ. MI.
315
CORREL. UNIT
317
L2 P-CHANNEL
CA-CODE UNIT
326
32
324
CARRIER GEN.
CODE DEL-LIN
CODE OUT
CORR CTL OUT
322
328
IQ0
IQ7
INPUT SELECTOR
IMAGE REJ-MI
325
CORR. UNIT
327

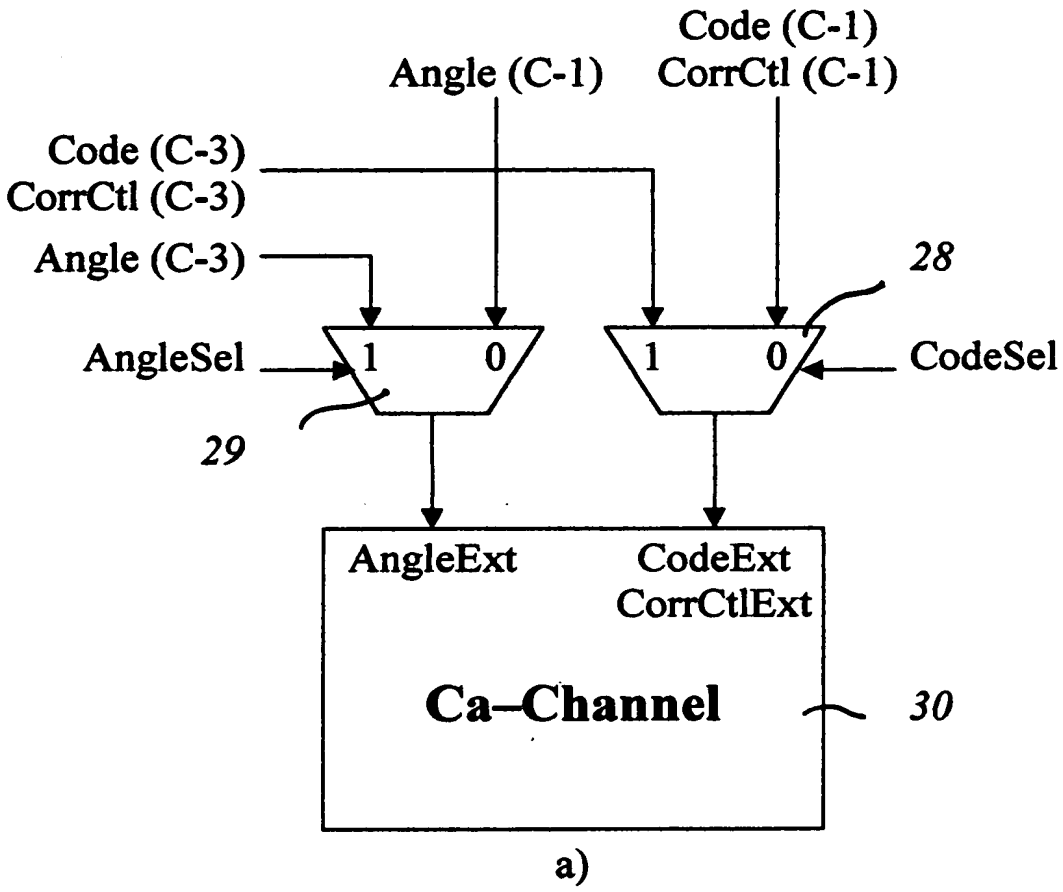
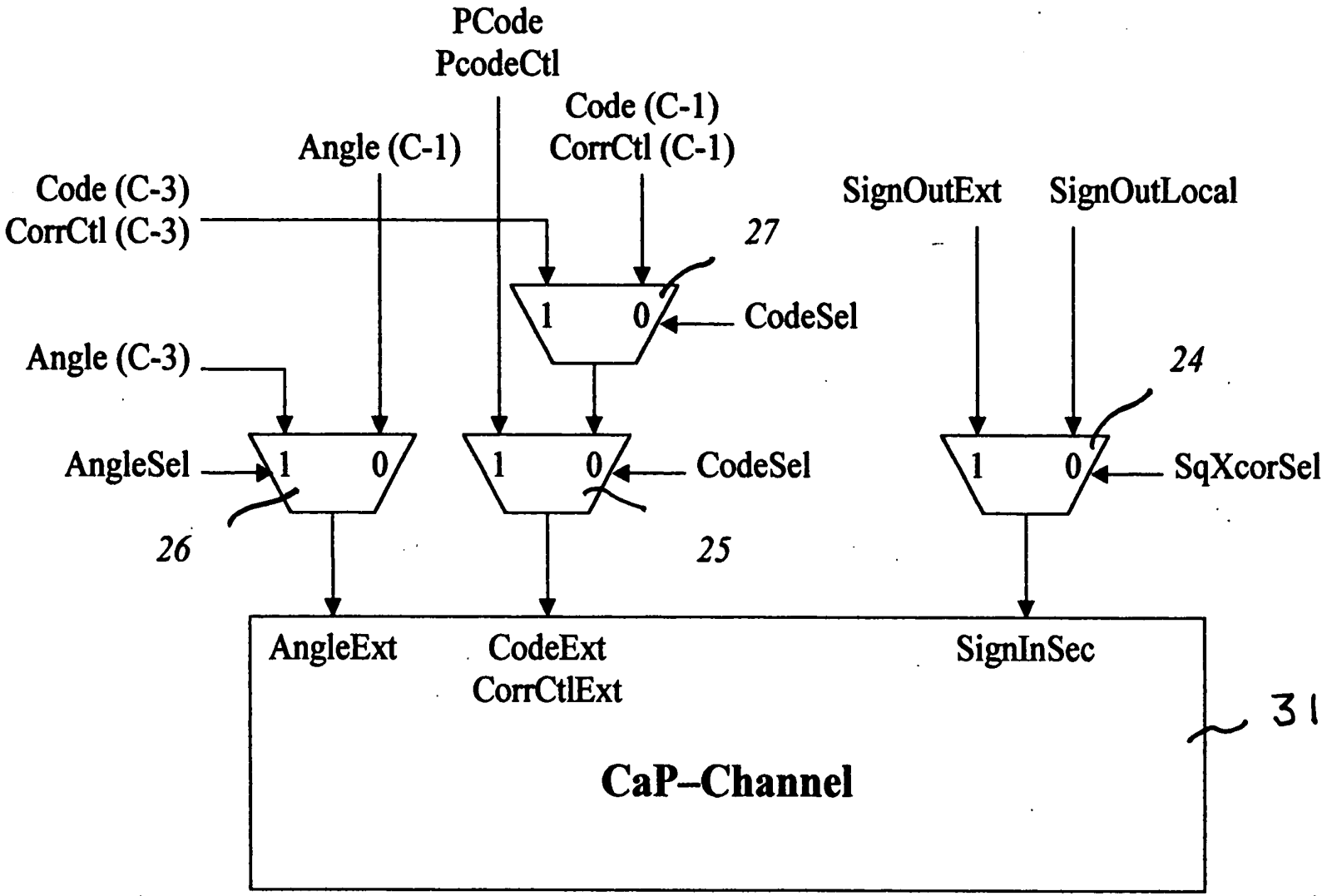

Code (C-1)
Angle (C-1)
CorrCtl (C-1)
Code (C-3)
CorrCtl (C-3)
Angle (C-3)
28
AngleSel
1
0
1
0
CodeSel
29
AngleExt
CodeExt
CorrCtlExt
Ca–Channel
30
a)

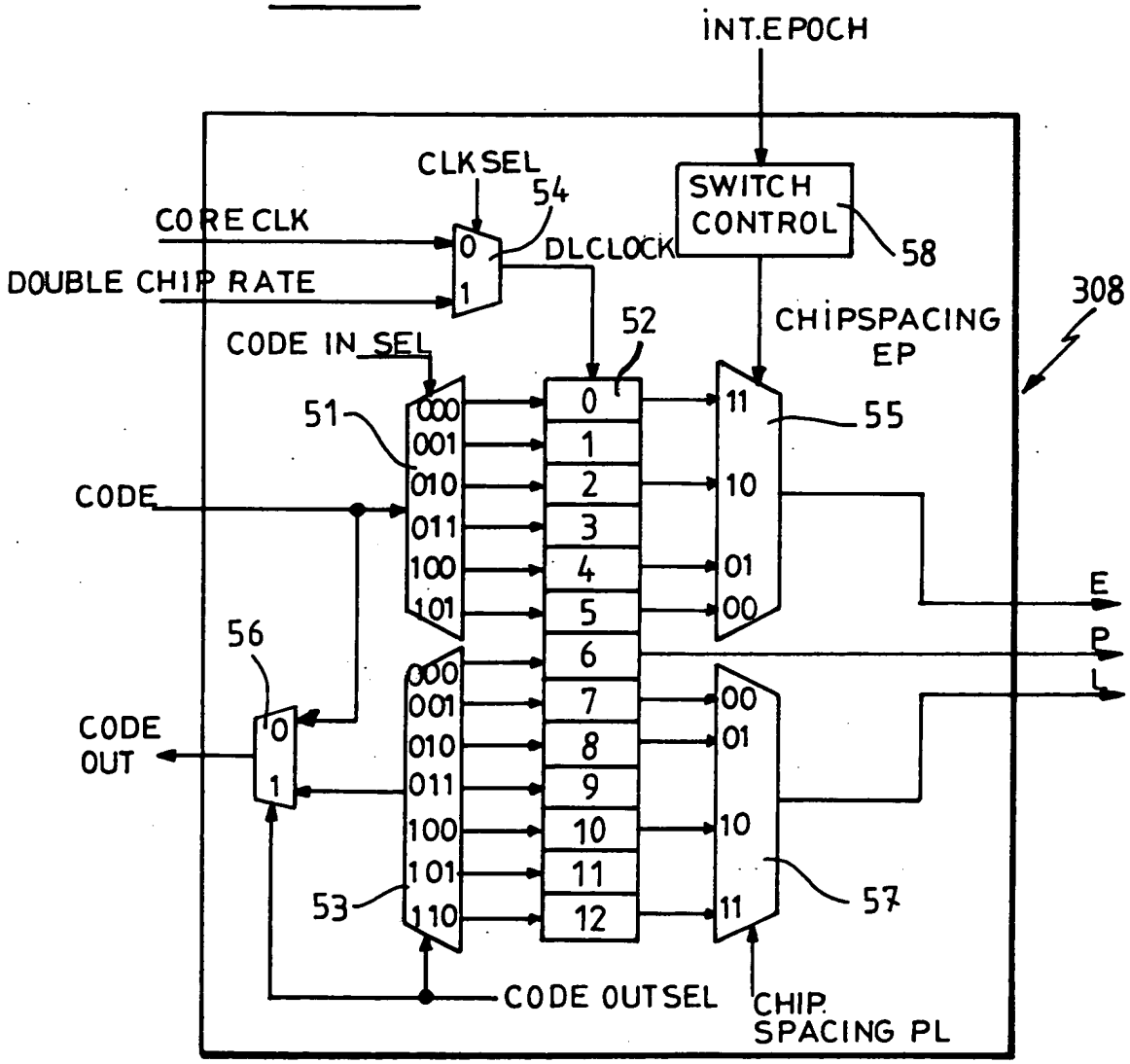
Fig. 7a

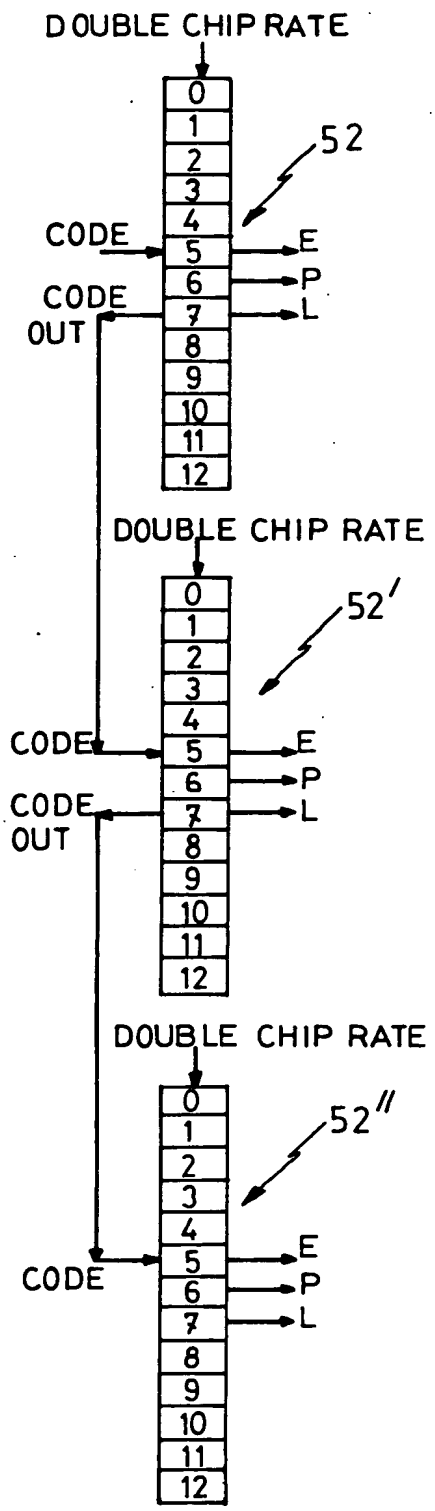

PCode
PcodeCtl
Code (C-1)
CorrCtl (C-1)
Angle (C-1)
Code (C-3)
CorrCtl (C-3)
SignOutExt
SignOutLocal
27
1
0
CodeSel
Angle (C-3)
24
AngleSel
1
0
1
0
CodeSel
1
0
SqXcorSel
26
25
AngleExt
CodeExt
CorrCtlExt
SignInSec
31
CaP–Channel

b)

Fig. 7b

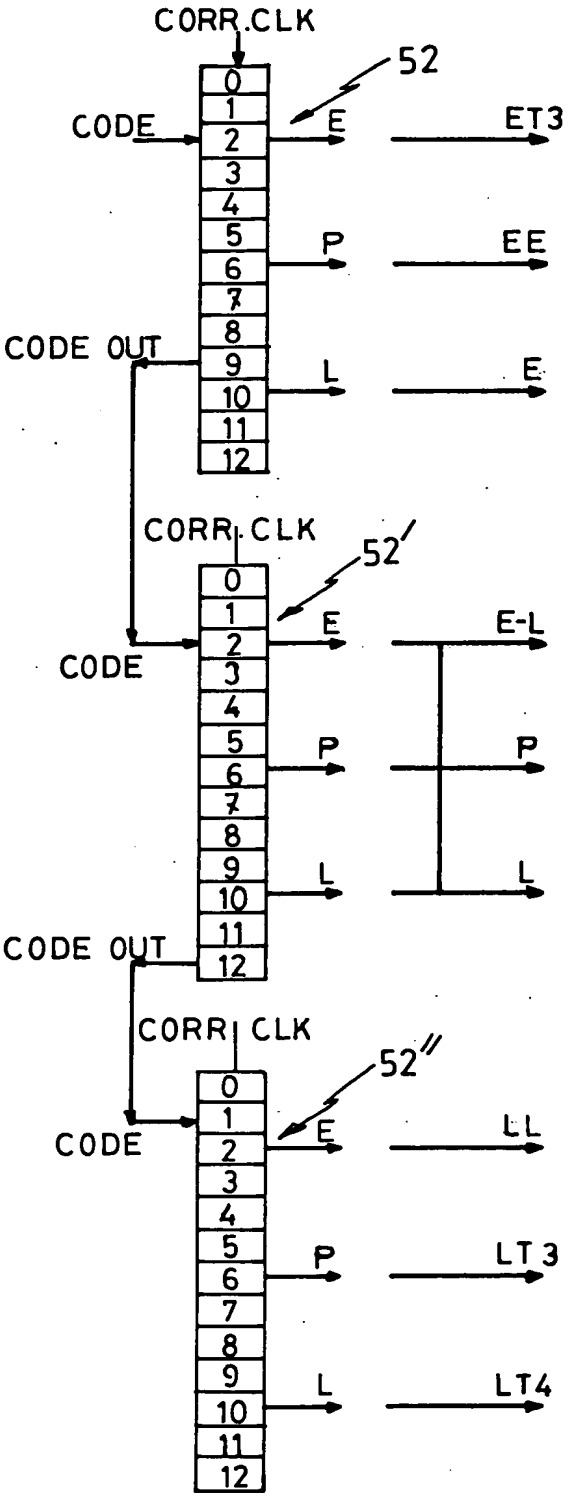
FIG. 8


INT.EPOCH
CLKSEL
54
SWITCH CONTROL
58
CORE CLK
DOUBLE CHIP RATE
DLCLOCK
308
CHIPSPACING EP
52
CODE IN_SEL
51
000
001
010
011
100
101
CODE
0
1
2
3
4
5
6
7
8
9
10
11
12
11
10
01
00
55
E
P
L
56
CODE OUT
53
00
01
10
11
57
CODE OUTSEL
CHIP SPACING PL



(a)FAST ACQUISITION MODE

FIG. 9a



(b)MULTIPATH MITIGATION WITH 8T SPACING BETWEEN E AND L

FIG. 9b

8661TT 85961160

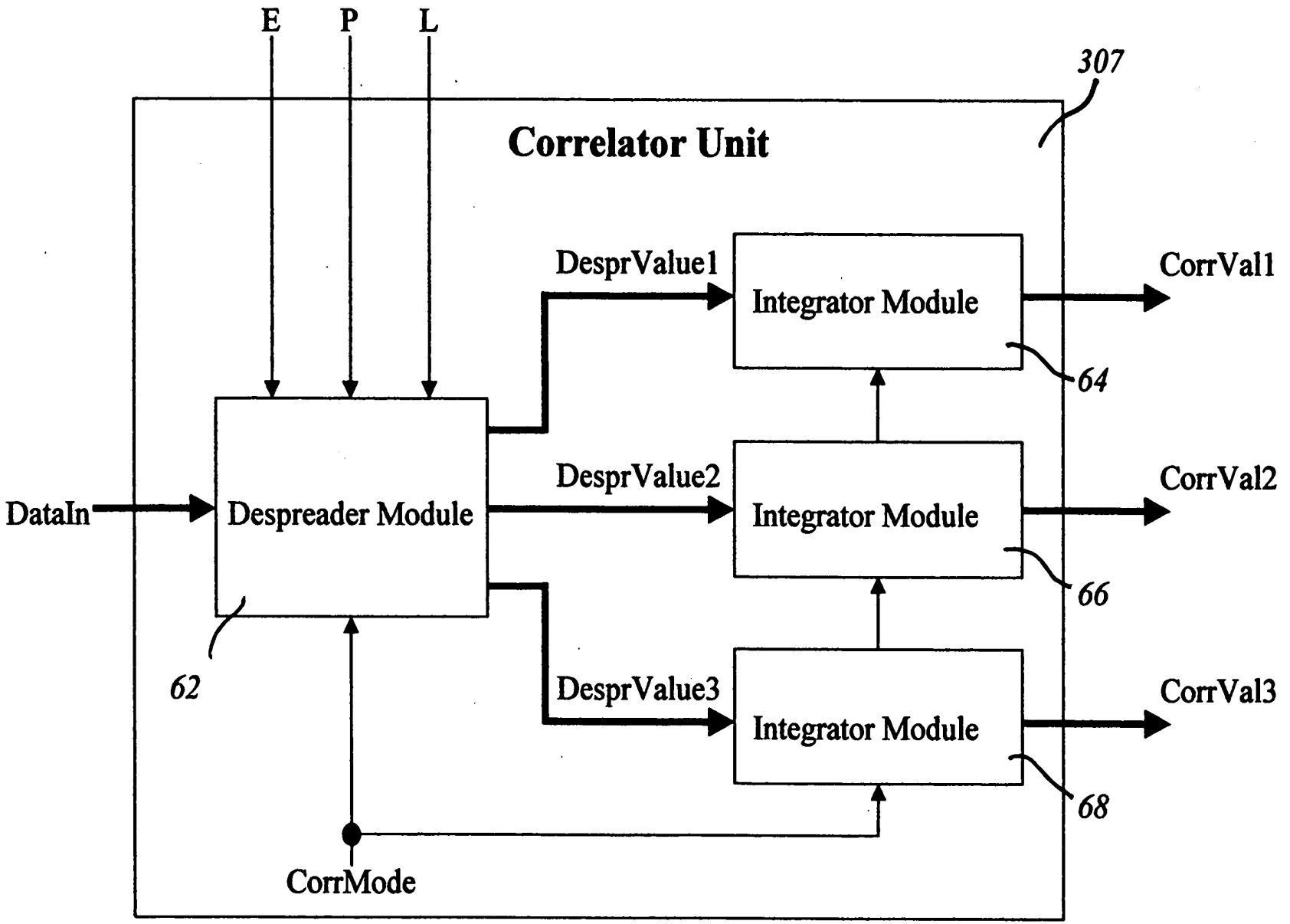


Fig. 10

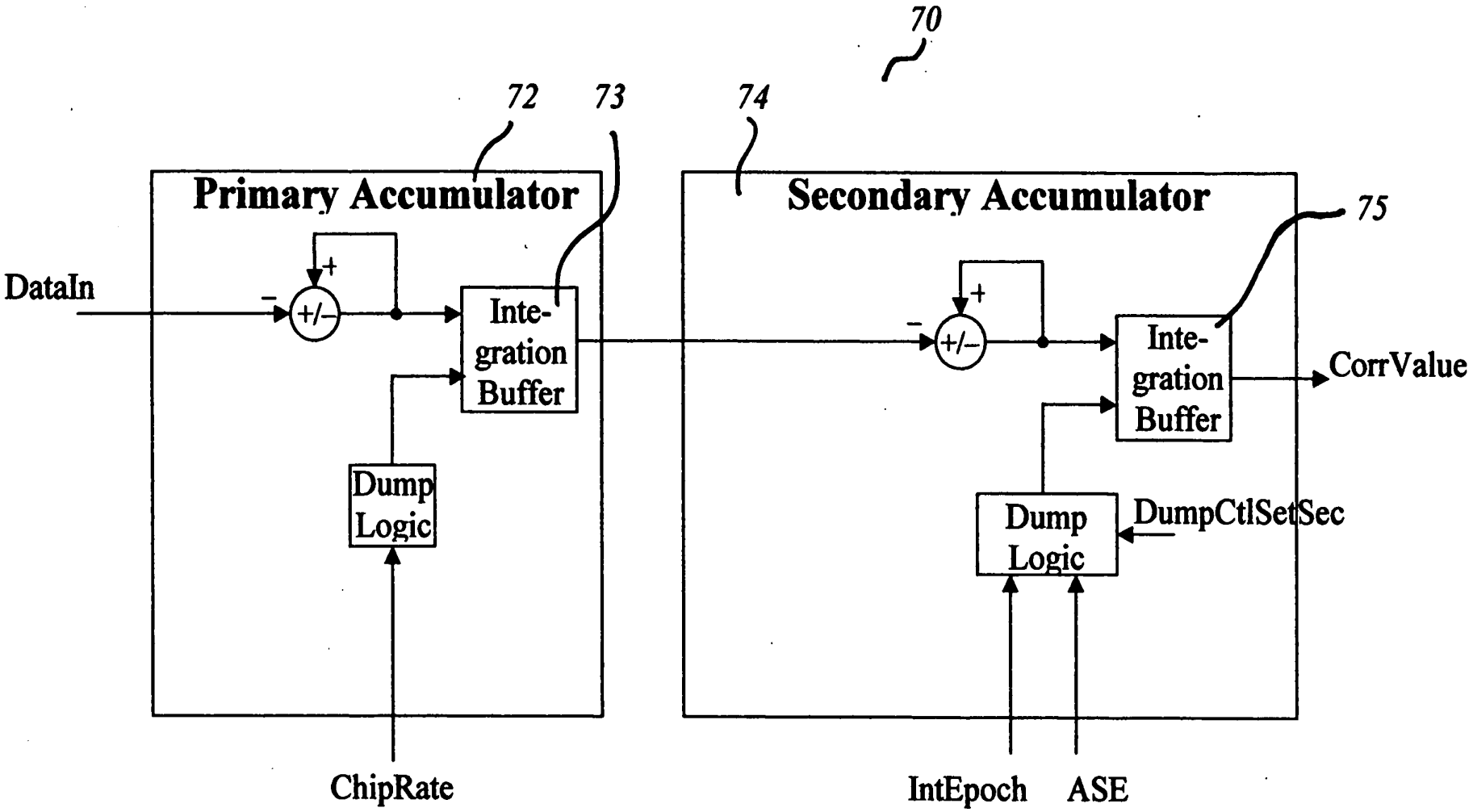

70
72
73
74
75
Primary Accumulator
Secondary Accumulator
DataIn
+
−
+/−
Inte-
gration
Buffer
Dump
Logic
CorrValue
DumpCtlSetSec
ChipRate
IntEpoch
ASE

Fig. 11

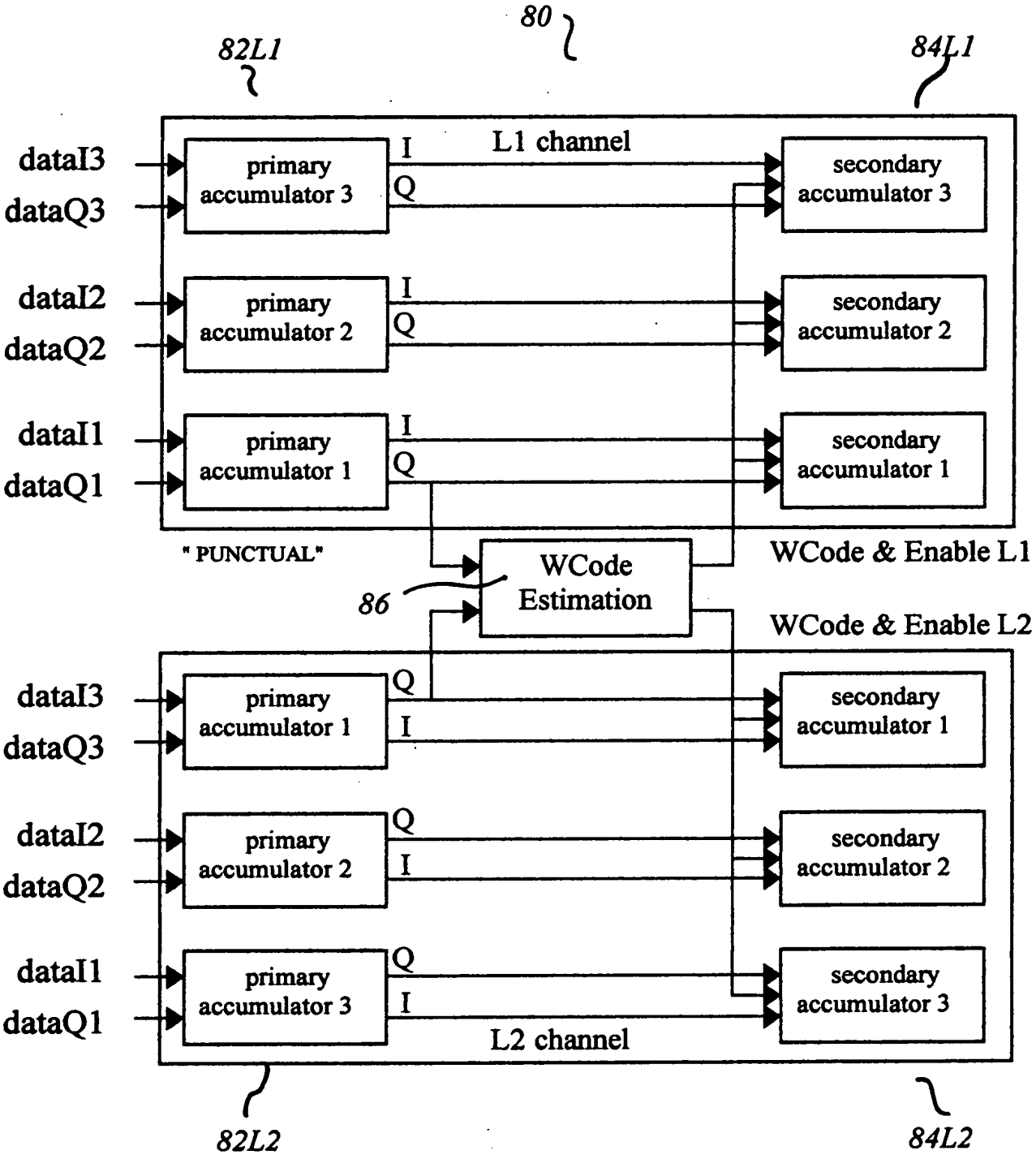

80
82L1
84L1
L1 channel
dataI3
dataQ3
primary accumulator 3
I
Q
secondary accumulator 3
dataI2
dataQ2
primary accumulator 2
secondary accumulator 2
dataI1
dataQ1
primary accumulator 1
secondary accumulator 1
" PUNCTUAL"
WCode Estimation
86
WCode & Enable L1
WCode & Enable L2
L2 channel
82L2
84L2

Fig. 13

866TTT"8596T60

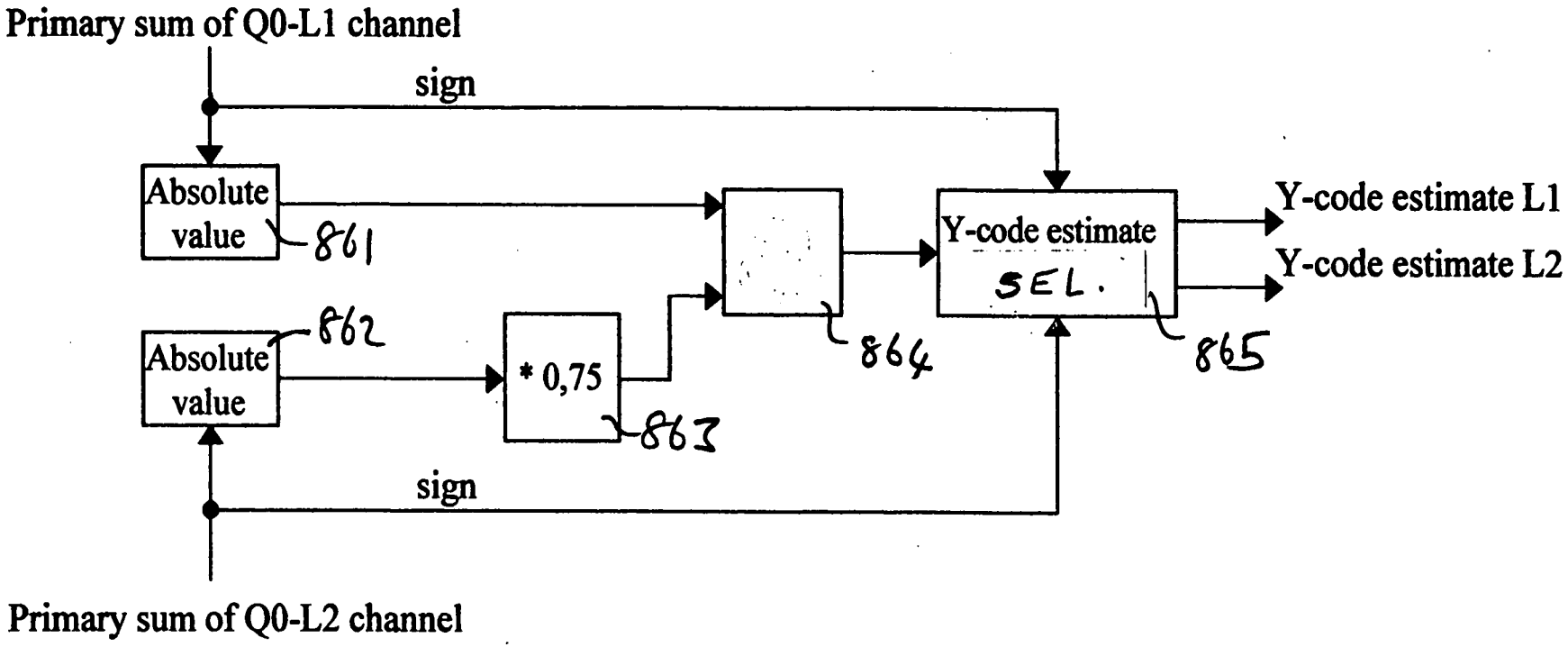


Fig. 14

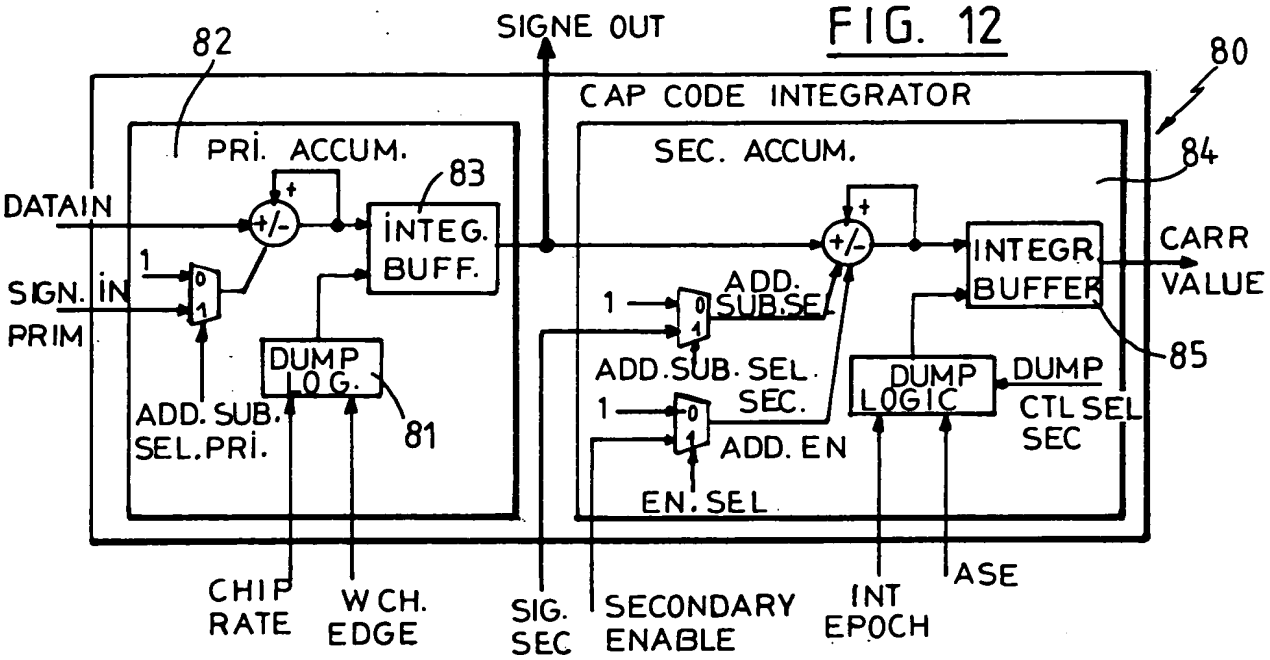

SIGNE OUT
82
80
CAP CODE INTEGRATOR
PRI. ACCUM.
SEC. ACCUM.
84
83
DATAIN
INTEG. BUFF.
INTEGR BUFFER
CARR VALUE
SIGN. IN PRIM
ADD. SUB. SEL
DUMP LOG.
81
ADD. SUB. SEL. PRI.
ADD. SUB. SEL. SEC.
DUMP LOGIC
DUMP CTL SEL SEC
85
ADD. EN
EN. SEL
CHIP RATE
W CH. EDGE
SIG. SEC
SECONDARY ENABLE
INT EPOCH
ASE

FIG. 12

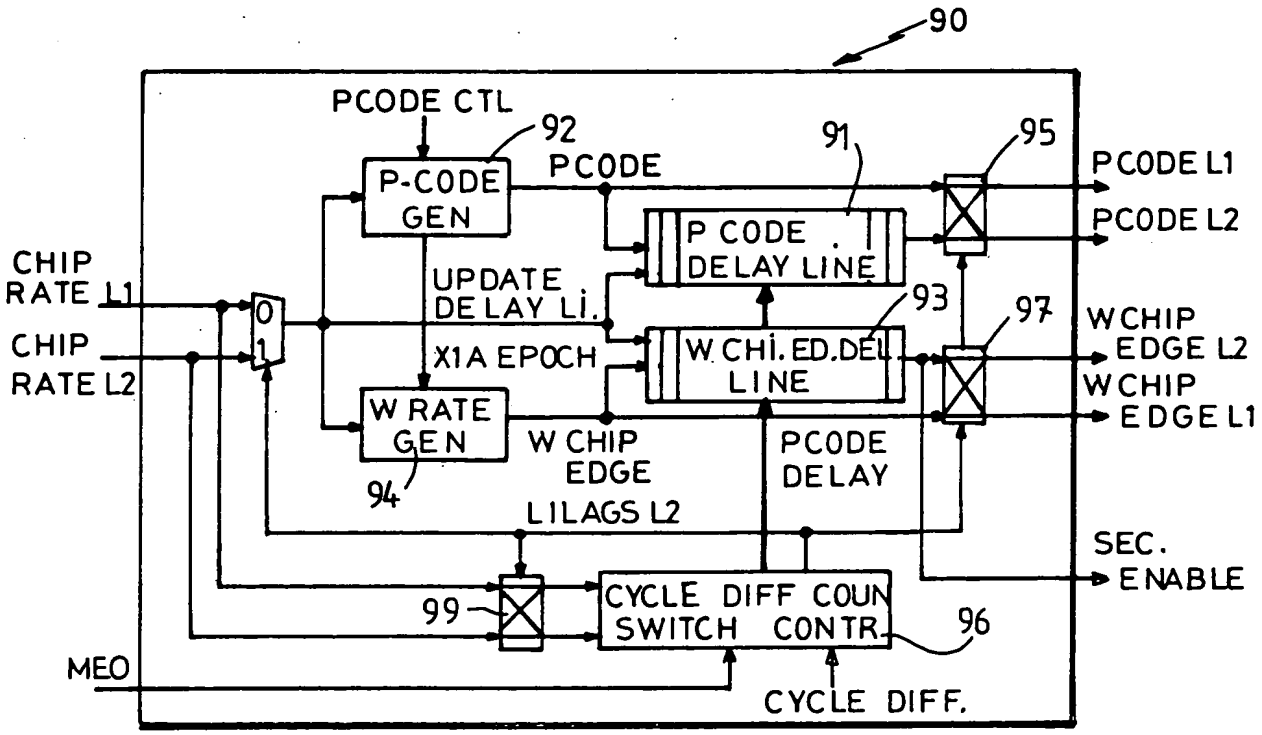

90
PCODE CTL
92
P-CODE GEN
PCODE
91
95
PCODE L1
PCODE L2
P CODE DELAY LINE
CHIP RATE L1
CHIP RATE L2
UPDATE DELAY LI.
93
97
W CHIP EDGE L2
W CHI. ED. DEL LINE
X1A EPOCH
W CHIP EDGE L1
W RATE GEN
94
W CHIP EDGE
PCODE DELAY
LILAGS L2
SEC. ENABLE
99
CYCLE DIFF COUN SWITCH CONTR
96
MEO
CYCLE DIFF.

FIG. 15